Final Exam

(December 9th @ 7:00 pm)
Clarity is very important! Show your procedure!

PROBLEM 1 (15 PTS)

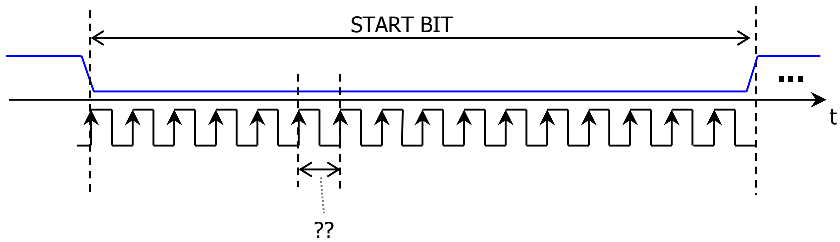
- Determine whether the following statements are True or False. If the statement is False, explain why.
  - ✓ HCS12D SCI1: With E-clock = 24 MHz, it is possible for the frequency of the receiver clock to be 2560 Hz.
  - ✓ CAN: The Bit Rate of System A is identical to that of System B. The CAN Bit Time of System A is 8 time quanta, and the CAN Bit Time of System B is 10 time quanta. Thus, the CAN Bit Time (in units of time) of System A is different to that of System B.
  - ✓ The Real-Time Interrupt can be disabled by setting bit I of CCR to '1'.
  - ✓ HCS12D CAN: Hard Synchronization takes place at the beginning of the frame, when the start of frame bit changes the state of the bus from dominant (0) to recessive (1).
  - ✓ `/XIRQ` Interrupt: A user can always disable it at any time during program execution by setting bit X of CCR to '1'.
  - ✓ HCS12D SCI1: The receiver clock is 16 times faster than the transmitter clock to allow for synchronization.
- Complete:
  - ✓ HCS12D ATD0, V_{DD} = 5v: The minimum number of bits that makes sure that the average quantization error never exceeds 0.001v is ________.
  - ✓ HCS12D Timer with E-clock= 24 MHz and pre-scale factor 8: A count from 0 to the maximum count lasts _________ ms.
  - ✓ HCS12D SPI0: If E-clock = 24 MHz and `SPI0BR = 0x57`, the Baud Rate is ____________ Hz.
- Miscellaneous questions:
  - ✓ PWM signal generation: Mention one advantage of using the PWM Module instead of the Output Compare function?
  - ✓ CAN: What is bit stuffing?
  - ✓ HCS12 Timer: Briefly describe the Input Capture function.
  - ✓ When servicing an Interrupt, the HCS12 stores PC and CPU registers in the Stack. What information does the PC register contain?
- Mark the correct option:
  - ✓ At power-on, the `/IRQ` Interrupt is: <u>Disabled</u> <u>Enabled</u>
  - ✓ HCS12D: Which of these two can be modified by the user? <u>Interrupt Vector</u> <u>Vector Address</u>

PROBLEM 2 (10 PTS)

- HCS12D – SCI1: Complete the table. E-clock = 24 MHz.

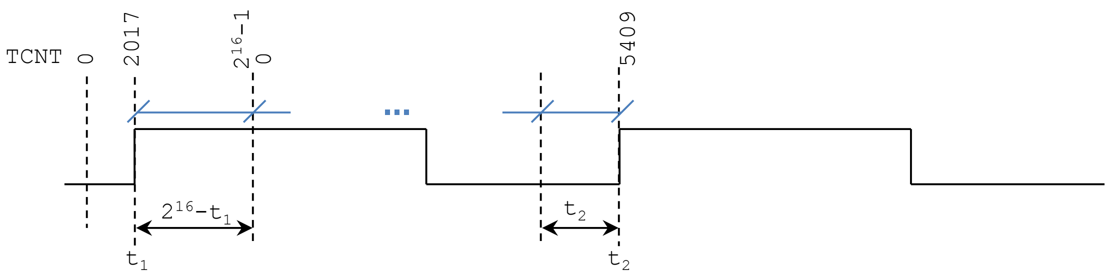
Baud Rate = Tx clock frequency (Hz)	**Rx clock frequency** (Hz)	**SCI1BDH**	**SCI1BDL**
2000			

- The figure below depicts the process of detection of a Start Bit. Using the parameters above, determine the period of the clock signal in the figure below.



PROBLEM 3 (20 PTS)

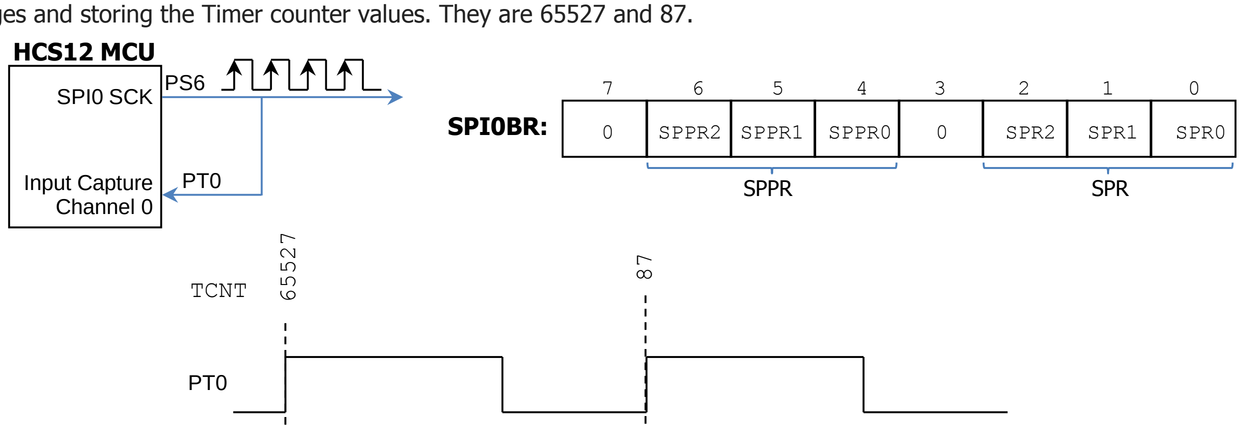
- (10 pts) HCS12D Timer: A program measures the period of a signal by using the Input Capture function and reading the TCNT values of two consecutive edges. In particular, the following values were read: 2017 and 5409.



The program also records the number of Timer overflows (rolling from `$FFFF` to `$0000`). In this particular case, the Timer overflows 3 times between t_1 and t_2.

✓ What is the frequency of the signal? E-clock = 24 MHz, Timer Pre-scale Factor = 4.

- (10 pts) HCS12D Timer and SPI Unit: We want to measure the clock frequency of the SPI unit with the Timer. To this end, we wire the SPI Clock (SCK) to an Input Capture Channel. We measure the SCLK period by detecting 2 consecutive rising edges and storing the Timer counter values. They are 65527 and 87.



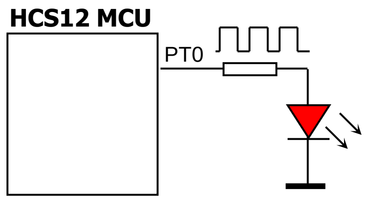
$$SPI\ SCK = Baud\ Rate = \frac{E-clock}{Baud\ Rate\ Divisor},\ Baud\ Rate\ Divisor = (SPPR+1)\times 2^{(SPR+1)}$$

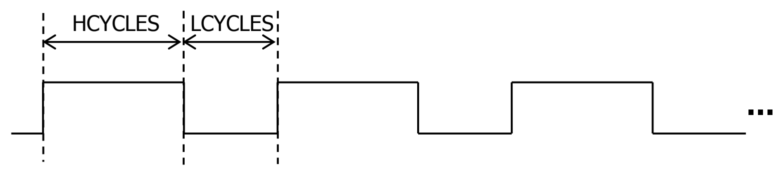
✓ What are the minimum and maximum attainable periods (in units of time) for the SPI clock?
✓ What is the Baud Rate (and the value of `SPI0BR`) of the SPI Unit? Hint: Consider the range of possible SPI clock periods to determine the number of times the Timer Counter rolls from `$FFFF` to `$0000`. E-clock = 24 MHz. Timer Pre-scale Factor = 2.

PROBLEM 4 (20 PTS)

- Assuming that brightness is proportional to the duty cycle of a square waveform, a PWM signal can control the brightness of an LED. We want to dim the LED brightness in the following manner:
  - 1 second at 95% intensity, 1 second at 60% intensity, 1 second at 45% intensity, 1 second at 30% intensity, and 1 second at 4% intensity

- We use the Timer Output Compare Channel 0 to generate 80Hz square waveforms with different duty cycles. The code requires us to specify HCYCLES and LCYCLES (in number of Timer cycles).





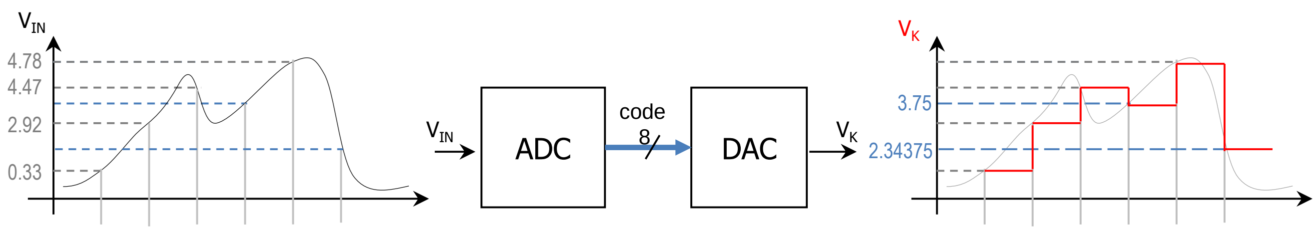
✓ Complete the following table, where the Timer Pre-scale factor must be maximized for each case. E-clock = 24 MHz.

Duty Cycle	HCYCLES	LCYCLES	Pre-scale Factor	Timer Clock Frequency
95%				
60%				
45%				
30%				
4%				

PROBLEM 5 (15 PTS)

- Analog to Digital Conversion: The figure depicts the process of converting 6 consecutive analog values. Using the successive approximation algorithm (when needed) and/or the formula for quantized voltage, complete the table below. V_{DD}=5v.

Formula for Quantized voltage: $V_k = \left(\frac{k}{2^n}\right) V_{DD}$



V_{IN} (v)	8-bit code	$V_k(v)$
0.33	00010000	
2.92		
4.47	11100100	
3.76		3.75
4.78		
2.35		2.34375

PROBLEM 6 (20 PTS)

A CAN system has the following characteristics:

- Bit rate = 500 kbps Bus length = 100 m
- Bus propagation delay = $4 \times 10^{-9}\,{}^{s}/_{m}$
- Transmitter (MCP2551 Transceiver) plus receiver propagation delay = 150 ns at 85 ºC

- HCS12 CAN Module: E-clock = 24 MHz, Oscillator clock = 8 MHz. Pre-scale factor = `CANnBTR0 (5..0)`. The CAN clock source is selected by `CANnCTL1(6)`.

- Calculate: i) CAN Pre-scale factor, ii) Time Quantum, iii) CAN Bit Time (in units of time and in time quanta), and iv) Time segments (in time quanta) for the following cases:

sync_seg	prop_seg	phase_seg1	phase_seg2

  - ✓ `CANnCTL1(6) = 0`. Clock Source: Oscillator Clock
  - ✓ `CANnCTL1(6) = 1`. Clock Source: E-clock